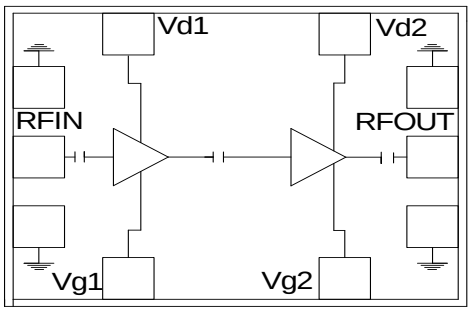
11 - 15 GHz 0.5 Watt Power Amplifier

Features

- **Frequency Range : 11 - 15GHz**
- **27.5 dBm output Psat**
- **13 dB Power gain**
- **25% PAE**
- **High IP3**
- **Input Return Loss > 11 dB**
- **Output Return Loss > 6 dB**
- **Dual bias operation**
- **No external matching required**
- **DC decoupled input and output**
- **0.15 µm InGaAs pHEMT Technology**
- **Chip dimension: 2.4 x 1.7 x 0.1 mm**

Functional Diagram



Typical Applications

- **RADAR**
- **Military & space**
- **LMDS, VSAT**

Description

The ASL4029 is a Ku-band Power amplifier with 0.5 watt power output. The PA uses 2 stages of amplification and operates in 11 - 15 GHz frequency range. The PA features 13 dB of gain with input and output return losses of 11 dB and 6 dB respectively. The PA has a high IP3 of 36dBm and 25% PAE. The chip operates with dual bias supply voltage.The die is fabricated using a reliable 0.15µm InGaAs pHEMT technology. The Circuit grounds are provided through vias to the backside metallization.

Absolute Maximum Ratings (1)

Parameter	Absolute Maximum	Units
Drain bias voltage (Vd)	+6	volts
Drain current (Idq)	500	mA
RF input power (RFin at Vd=9V)	23	dBm
Operating temperature	-50 to +85	°C
Storage Temperature	-65 to +150	°C

1. Operation beyond these limits may cause permanent damage to the component

Electrical Specifications (1) @ T_A = 25 °C, V_{d1} = V_{d2} = 5V, V_{g1} = V_{g2} = -0.65V
Z_o =50 Ω

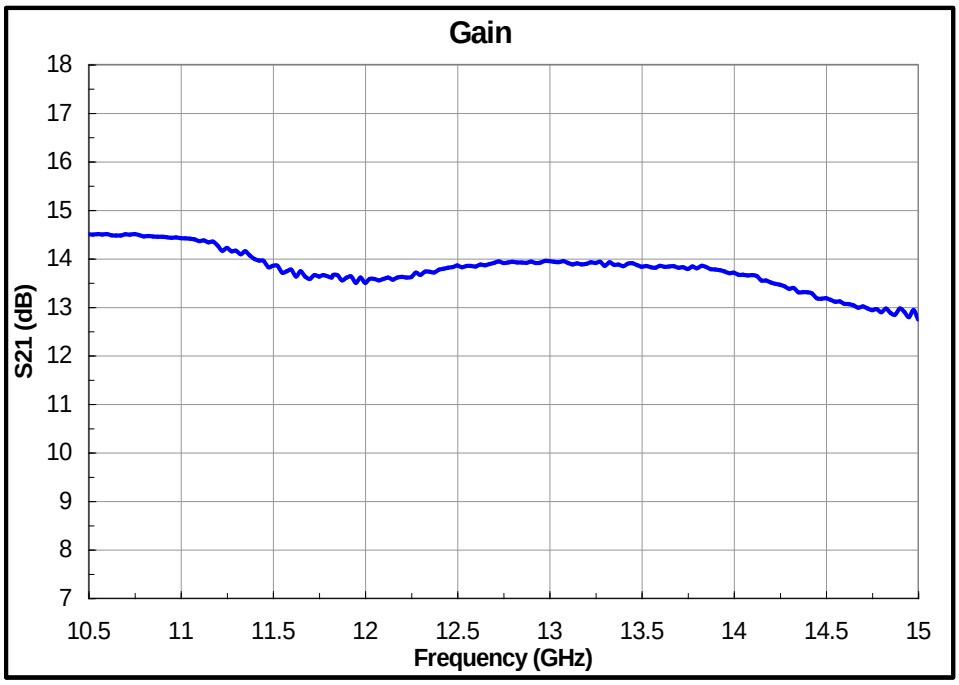
Parameter	Typ.	Units
Frequency Range	11 - 15	GHz
Gain	13	dB
Gain Flatness	+/-0.6	dB
Output Power (P1 dB)	26.5	dBm
Input Return Loss	11	dB
Output Return Loss	6	dB
Saturated output power (Psat)	27.5	dBm
Output Third Order Intercept (IP3)	36	dBm
Power Added Efficiency (PAE)	25%	--
Supply Current (Idq)	300	mA
Saturated current (Id_{sat})	500	mA

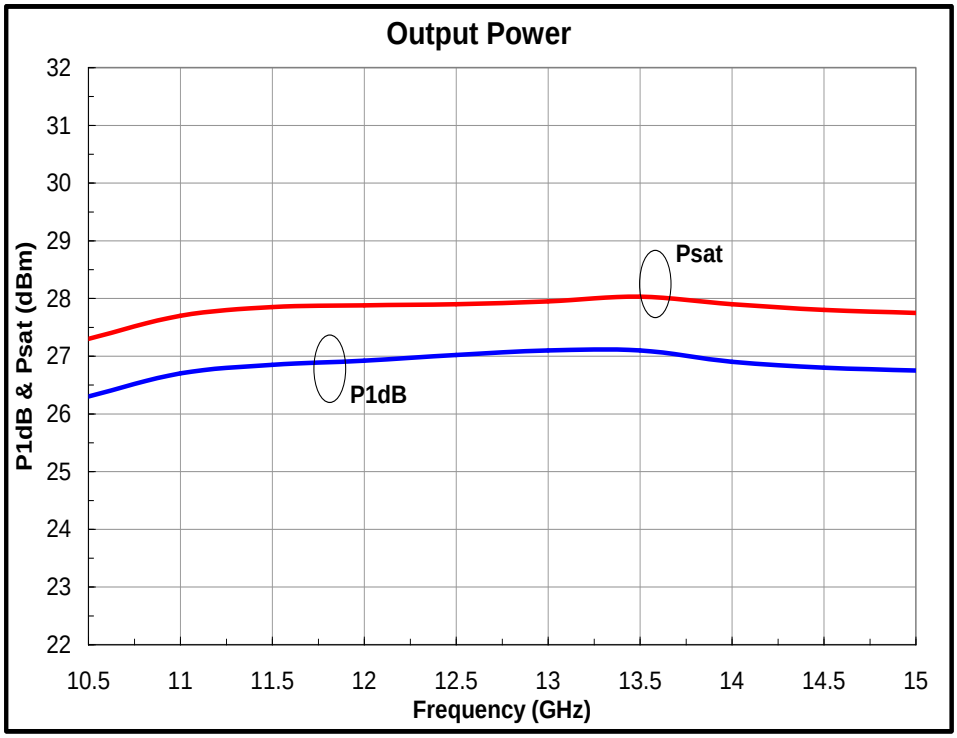
Note:

1. Electrical specifications as measured in test fixture.

Test fixture data

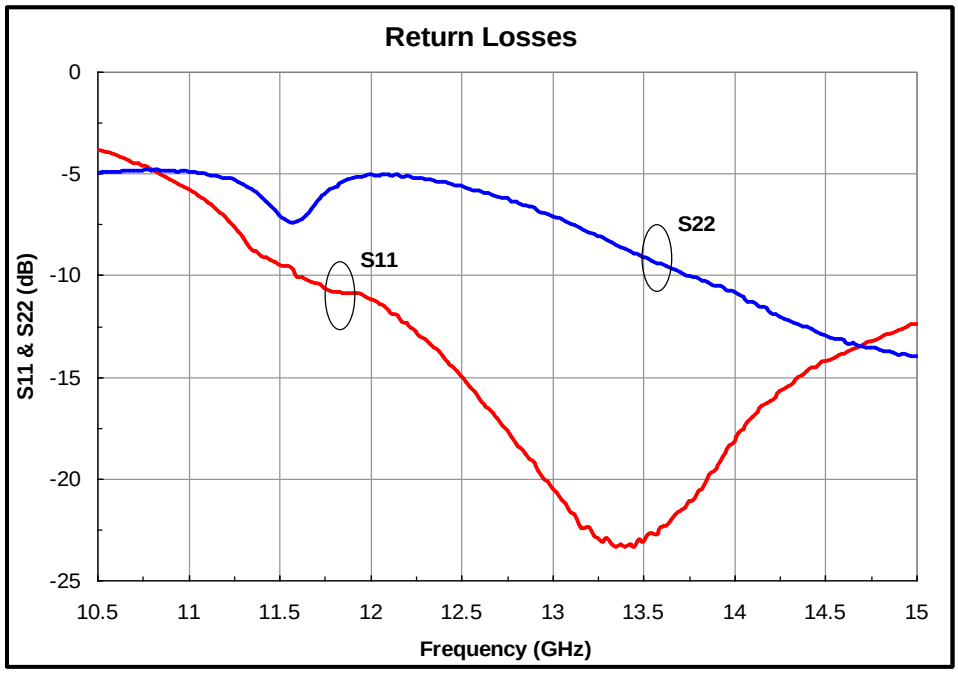
V_{d1} = V_{d2} = 5V, V_{g1} = V_{g2} = -0.65V, Total Current (Idq) =300ma, T_A = 25 °C

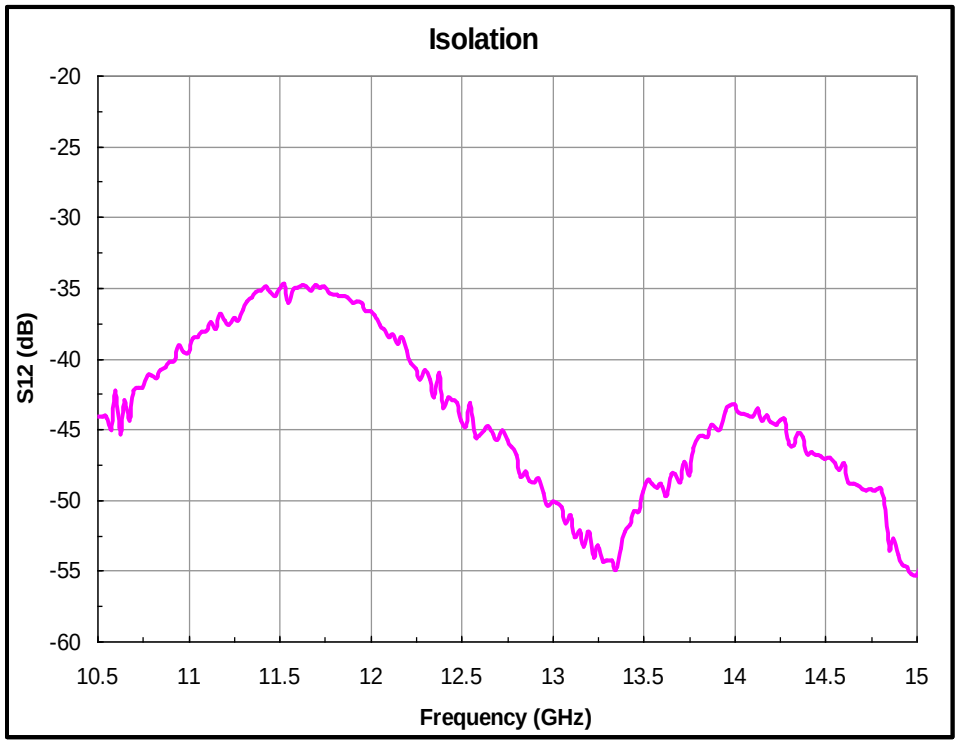




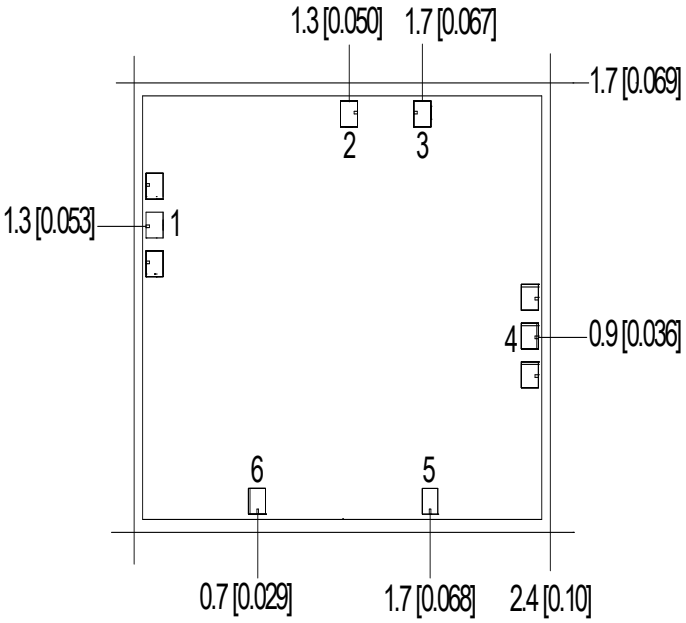
Test fixture data

V_{d1} = V_{d2} = 5V, V_{g1} = V_{g2} = -0.65V, Total Current (Idq) =300ma, T_A = 25 °C





Bond Pad Locations

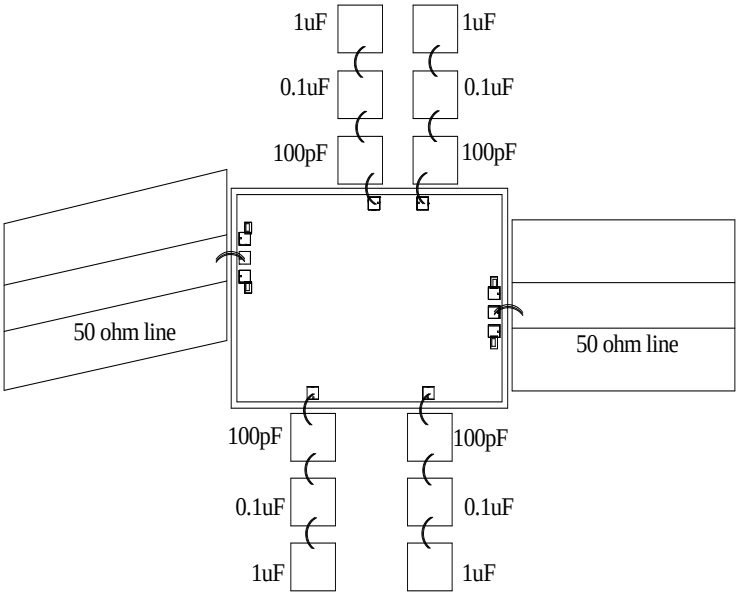


Units: millimeters (inches)

Note:

1. All RF and DC bond pads are 100µm x 100µm
2. Pad no. 1 : RF IN
3. Pad no. 2 : 1st stage drain voltage(V_{d1})
4. Pad no. 4 : RF Out
5. Pad no. 3 : 2nd stage drain voltage(V_{d2})
6. Pad no. 5 : 2^{nd} stage gate voltage(V_{g2})
7. Pad no. 6 : 1^{st} stage gate voltage (V_{g1})

Recommended Assembly Diagram



Note :

1. Two 1 mil (0.0254mm) bond wires of minimum length should be used for RF input and output.
2. Two 1 mil (0.0254mm) bond wires of minimum length should be used from chip bond pad to 100pF capacitor.
3. Input and output 50 ohm lines are on 5 mil RT Duroid substrate
4. 0.1 µF capacitors may be additionally used as a second level of bypass for reliable operation
5. The RF input & output ports are DC decoupled on-chip.
6. Proper heat sink like Copper tungsten or copper molybdenum to be used for better reliability of chip

Die attach: For Epoxy attachment, use of a two-component conductive epoxy is recommended. An epoxy fillet should be visible around the total die periphery. If Eutectic attachment is preferred, use of fluxless AuSn (80/20) 1-2 mil thick preform solder is recommended. Use of AuGe preform should be strictly avoided.

Wire bonding: For DC pad connections use either ball or wedge bonds. For best RF performance, use of 150 - 200µm length of wedge bonds is advised. Single Ball bonds of 250-300µm though acceptable, may cause a deviation in RF performance.

GaAs MMIC devices are susceptible to Electrostatic discharge. Proper precautions should be observed during handling, assembly & testing

All information and Specifications are subject to change without prior notice